(2)

(19) Japanese Patent Office (JP)

(11) Patent Application Publication

(12) Laid-Open Patent Publication (A) Sho 63-239676

(51) Int. Cl.[4]	Identification Code	Office File No.	(43) Publication: October 5, 1988
G11C 11/34	362	G-8522-5B	

Examination request: Not requested

No. of inventions: 1

(Total of 14 pages)

---

(54) Title of the Invention: Semiconductor memory device

(21) Patent Application: Sho 62-71428

(22) Application: March 27, 1987

(72) Inventor: Yasunori [N.B. Other readings of first name possible.] Yamaguchi
c/o Hitachi, Ltd., Device Development Center
2326 Imai, Ome-shi, Tokyo

(71) Applicant: Hitachi, Ltd.
4-6 Kanda-surugadai, Chiyoda-ku, Tokyo

(74) Agent: Patent agent Masao [N.B. Other readings of first name possible.] Ogawa and one other

Specifications

1. Title of the invention

Semiconductor memory device

2. Claims

1. A semiconductor memory device comprising:

a serial-parallel conversion circuit that receives a plurality of read data that is parallelly output over a plurality of data lines constituting a memory array and provides a serial output in accordance with a clock signal from an external source; and

a timing control circuit that controls the serial output operation of the aforesaid serial-parallel conversion circuit; and

characterized by:

the timing for starting the aforesaid serial output operation being set at will by specifying the number of cycles of the aforementioned clock signal required between activation by an activation control signal from an external source and the start of the aforementioned serial output operation.

2. A semiconductor memory device described in claim 1 characterized by the aforesaid timing control circuit comprising:

a counter circuit that obtains the aforesaid number of cycles from an external source in synchrony with the aforementioned activation control signal and then performs a count-down operation in accordance with the aforementioned clock signal; and

a timing generation circuit which, upon detection of logical "0" for all bits in the output signal of the aforementioned counter circuit, creates an internal clock signal that is used for a serial output operation.

3. A semiconductor memory device described in claim 1 or claim 2 characterized by:

the aforementioned semiconductor memory device being a dual port memory; and

the aforementioned number of cycles being provided over a plurality of data input/output terminals for random access port use.

3.Detailed description of the invention

Field of industrial use

The present invention relates to semiconductor memory devices and in particular to an art that is effective, for example, when used with a dual port memory that is used for image processing and possessing both a random input/output function and a serial input/output function.

Prior art

A description of a frame buffer memory used with images to display characters, graphics, etc. on a CRT (cathode ray tube) screen is found, for example, in pages 243 through 264 of "Nikkei Electronics" dated March 24, 1986 published by Nikkei McGraw-Hill.

The dual port memory described in the aforesaid literature is provided with a random access port that is used for the input and output of memory data in one-bit units or several-bit units, and a serial access port that is used for the serial input and output of memory data in units of word lines in a memory array.

Problems to be solved with the present invention

As Fig. 4 shows, a dual port memory such as the above is provided with, as external control signals, row address strobe signal $\overline{RAS}$, column address strobe signal $\overline{CAS}$ and write enable signal $\overline{WE}$ and additionally, for example, data transfer control signal $\overline{DT}/\overline{OE}$, serial output control signal $\overline{SOE}$ and serial clock signal SC. With a dual port memory, the read data transfer mode – where the read data is serially output – is recognized when the levels of the column address strobe signal $\overline{CAS}$ and write enable signal $\overline{WE}$ are high and the level of the data transfer control signal $\overline{DT}/\overline{OE}$ is low when the level of the row address strobe signal $\overline{RAS}$ changes from high to low At this time, the

address AX of the word line to be read is provided to external terminals A0 through Ai in synchrony with the level of the row address strobe signal $\overline{RAS}$ rising to high, and the read signals from the memory cells that are connected to the selected word line are set up in the data lines. Also, in synchrony with the level of the column address strobe signal $\overline{CAS}$ falling to low which occurs with a slight delay following the level of the row address strobe signal $\overline{RAS}$ becoming low, the address AY of the first column that is to be serially output is supplied to external terminals A0 through Ai.

Thereafter, when the level of the data transfer control signal $\overline{DT}/\overline{OE}$ is set back to high, timing signal ϕdt is generated – the timing signal ϕdt is used to transfer to the data register of the serial access port the read data that had been parallelly output to each of the data lines – and, along with that, an output operation is begun for the new serial data (data following (AX·AY)) that had been transferred to the data register in accordance with the timing signal ϕc which is generated in synchrony with the serial clock signal SC.

After the level of the data transfer control signal $\overline{DT}/\overline{OE}$ is once set to low, the serial output operation begins when the level returns to high. The timing for this is controlled by monitoring the output signal of a counter circuit which counts the horizontal pixel location and which is provided in an external memory control circuit that drives the said dual port memory. To explain, when the output of the read data in the memory cells that are connected to one word line in a dual port memory is near completion, the dual port memory is reactivated and the read data in the memory cells of the new word line is output to the corresponding data lines. Thereafter, the level of the data transfer control signal

$\overline{DT}/\overline{OE}$ is returned to high while monitoring when the level of the serial clock signal SC becomes low which happens when the value of the counter circuit in the memory control circuit shows the end of the serial output operation for the read data from the memory cells connected to the preceding word line that had been selected. This then causes the read data in the memory cells that are connected to the newly selected word line to be transferred to the data register and initiates a serial output operation. This allows a real time data transfer in synchrony with the CRT's dot rate.

However, improvements in display technology have resulted in the development of high-resolution CRTs which have increased the dot rate that determines the rate at which display data is serially output. This has resulted in a difficulty in maintaining a synchrony between the rising of the level of the data transfer control signal $\overline{DT}/\overline{OE}$ and the serial clock signal SC. To explain, as described earlier, the timing for returning the level of the data transfer control signal $\overline{DT}/\overline{OE}$ to high is determined by monitoring the output signal of the counter circuit in the memory control circuit. This means that as the delay time involved in advancing the counter circuit using the serial clock signal SC, and the delay time involved in decoding and monitoring the output signal from the counter circuit begin to increase relative to the period of the serial clock signal SC, raising the level of the data transfer control signal $\overline{DT}/\overline{OE}$ in synchrony with the serial clock signal SC becomes difficult. As the dotted line in Fig. 4 shows, this results in a timing mismatch between the data transfer control signal $\overline{DT}/\overline{OE}$ and the serial clock signal SC, and in particular, a delay in the level of the data transfer control signal $\overline{DT}/\overline{OE}$ rising with respect to the rise in the level of the serial clock signal SC. This

then results in shortening the duration of the timing signal ϕdt which is used for transferring to the data register the read data from the memory cells that are connected to the newly selected word line. This results in an unstable serial data transfer operation and a disruption of the displayed images.

It is the object of the present invention to provide a semiconductor memory device such as a dual port memory with a stable serial data transfer operation.

The aforementioned object and other objects of the present invention and its new features will become apparent from the description in the specification and the attached figures.

Means for solving the problems

The following is a brief description of an overview of a representative embodiment among the embodiments disclosed in the present application. To explain, during data transfer in a dual port memory, the timing for starting the transfer of data to the data register is set at will by specifying the number of clock signal cycles required between the activation of the data transfer cycle and the initiation of the transfer operation.

Operation

When the data transfer operation is about to start in a dual port memory, the aforesaid means allows the clock signal position where the data transfer operation is to begin to be specified at will in accordance with the counter value of a counter circuit in a memory control circuit. Furthermore, since a count-down counter circuit provided within a dual port memory is used to perform the transfer operation in synchrony with a clock signal, a semiconductor memory device such as a dual port

memory with a stabilized display data transfer operation is realized.

Embodiments

Fig. 2 shows a block diagram of one embodiment of a dual port memory where the present invention is applied. The respective circuit blocks shown in the said figure are typically formed on, although not restricted to, a single semiconductor substrate such as a single crystal silicon using semiconductor integrated circuit fabrication technology of the public domain.

The dual port memory of this embodiment is provided with a random access port that is accessed in units of 4 bits and whose basic structural element is a dynamic RAM, and a serial access port where memory data is serially input and output in units of a word line. This allows the dual port memory to engage in a series of serial input/output operations simultaneous with accesses made to the random access port. Also, although not restricted by this, a random input/output circuit RIO that is included in the random access port is provided with a logical operation circuit for performing raster operations, etc. A function control circuit that controls the said logical operation circuit is also provided. The logical operation circuit is provided with various operation functions such as logical multiplication and logical addition, and which operation to perform is specified with a [logical] operation code which is specified by particular combinations of the control signals which are input through external terminals A0 through A3 for the address signals.

The serial access port is provided with a serial input/output circuit SIO. Ordinarily, memory data corresponding to four memory arrays are simultaneously and serially input and output through four serial input/output terminals SIO1 through SIO4. However, a specific combination of [logical] operation codes can be used to specify the use as a memory with a x1 bit configuration wherein read

data that are output from the four memory arrays are alternately output from input/output terminal SIO1.

From an external device, in addition to row address strobe signal $\overline{RAS}$, column address strobe signal $\overline{CAS}$, write enable signal $\overline{WE}$ and other control signals which are used in ordinary dynamic RAMs, the dual port memory is provided with data transfer control signal $\overline{DT/OE}$ which is used for output control and for controlling the data transfer between the random access port and the serial access port, the serial output control signal $\overline{SOE}$ which is used for controlling the switching between input and output operations by the serial access port, and the serial clock signal SC which is used as a synchronization signal during serial input and output operations.

Although not restricted by this, this embodiment of the dual port memory is provided with four memory arrays, M-ARY1 through M-ARY4, and sense amplifiers SA1 through SA4 and column switches CSW1 through CSW4 which correspond to the respective memory arrays. A column address decoder RCD and a row address decoder RD, common to memory arrays M-ARY1 through M-ARY4, are also provided. A plurality of such address decoders may be provided depending on the arrangement of the memory arrays on a semiconductor substrate. Fig. 2 shows memory array M-ARY1 and its peripheral circuitry for illustration purposes.

In Fig. 2, memory array M-ARY1 comprises (m + 1) word lines that are arranged in a direction perpendicular to the said figure, (n + 1) sets of complementary data lines arranged in a direction horizontal with the said figure, and (m + 1) x (n + 1) pieces of memory cells which are located at the intersections of the said word lines and complementary data lines.

The dynamic memory cells which configure the memory array M-ARY1 are constructed of capacitors for data storage and MOSFETs for address selection. The gates of the MOSFETs for address selection for the (n + 1) pieces of memory cells that are arranged along the same row are connected to the corresponding word line. Each word line is furthermore connected to the row address decoder RD so that one word line that is specified by the X address signal AX0 through AXi is specified and selected.

The row address decoder RD decodes the complementary internal address signals ax0 through axi (here the internal address signal, for example, ax0 with the same phase and the internal address signal $\overline{ax0}$ with the opposite phase as the X address signal AX0 that is supplied from an external source are collectively represented as complementary internal address signal ax0; the same convention is used hereinafter) that are supplied by row address buffer RADB, selects one word line that is specified by the X address signals AX0 through AXi and sets the selection state level to high. The selection operation of a word line by the row address decoder RD is performed in accordance with the word line selection timing signal ϕx that is supplied by the timing control circuit TC.

The row address buffer RADB receives the row address signal from address multiplexer AMX, forms complementary internal address signals ax0 through axi and supplies the signals to the row address decoder RD. The dynamic RAM of this embodiment uses the so-called address multiplex method wherein the X address signals AX0 through AXi which specify the row address and the Y address signals AY0 through AYi which specify the column address are time-division multiplexed and supplied through the same external terminals A0 through Ai. The X address signals AX0 through AXi which are supplied from an external source as control signals are fed to external terminals A0

through Ai in synchrony with the level of the row address strobe signal $\overline{RAS}$ falling, and the Y address signals AY0 through AYi which are supplied from an external source as control signals are fed to external terminals A0 through Ai in synchrony with the level of the column address strobe signal $\overline{CAS}$ falling. Furthermore, the dynamic RAM of this embodiment is provided with an automatic refresh mode wherein data stored in the memory cells are read and rewritten using a prescribed period. Therefore, a refresh address counter REFC is provided to specify the word line to be refreshed in the automatic refresh mode.

In accordance with the timing signal ϕref which is provided by the timing control circuit TC, the address multiplexer AMX selects the X address signals AX0 through AXi that are supplied via external terminals A0 through Ai and the refresh address signals cx0 through cxi supplied by refresh address counter REFC and transfers the signals to row address buffer RADB as row address signals. To explain, when the level of the timing signal ϕref is low meaning an ordinary memory access mode, the address multiplexer AMX selects the X address signals AX0 through AXi that are supplied by an external device via external terminals A0 through Ai; when the level of the timing signal ϕref is high meaning an automatic refresh mode, the address multiplexer AMX selects the refresh address signals cx0 through cxi that are supplied by the refresh address counter REFC.

As afore-described, since the X address signals AX0 through AXi are supplied to external terminals A0 through Ai in synchrony with the falling level of the row address strobe signal $\overline{RAS}$, the row address signals are obtained by the row address buffer RADB in accordance with the timing signal ϕar which is generated by the timing control circuit TC by detecting the falling level of the row

address strobe signal $\overline{RAS}$.

The drains of the MOSFETs used for selecting the addresses of the memory cells that are formed along the same column in memory array M-ARY1 are connected to the corresponding complementary data line. One end of each complementary data line in memory array M-ARY1 is connected to the corresponding switch MOSFET of the column switch CSW1 and, furthermore, is selectively connected to the complementary common data line CD1 (here the noninverting signal line CD1 and inverting signal line $\overline{CD1}$ of the complementary common data line are collectively represented as complementary common data line CD0; the same convention is used hereinafter.).

The column switch CSW1 comprises (n + 1) pairs of switch MOSFETs which are connected to their corresponding complementary data lines. The other ends of these switch MOSFETs are commonly connected to the noninverting signal line CD1 or inverting signal line $\overline{CD1}$ which constitute the complementary common data line. This allows the column switch CSW1 to selectively connect (n + 1) sets of complementary data with common complementary data line CD1. The gates of the two switch MOSFETs in each pair which constitute the column switch CSW1 are commonly connected and are provided with the data line selection signal which is created by the column address decoder RCD for the random access port.

The column address decoder RCD for the random access port decodes the complementary internal address signals ay0 through ayi that are supplied by the column address buffer CADB, and, in accordance with the data line selection timing signal ϕyr supplied by the timing control circuit TC, forms the aforementioned data line selection signal which is then supplied to column switches CSW1

through CSW4.

The timing control circuit TC detects the falling level of the column address strobe signal $\overline{CAS}$ and generates the corresponding signal ϕac. In accordance with the signal ϕac, the column address buffer CADB receives and holds the Y address signals AY0 through AYi supplied through external terminals A0 through Ai and forms the complementary internal address signals ay0 through ayi which are then supplied to the column address decoder RCD for the random access port.

The other ends of each complementary data lines in memory array M-ARY1 are connected to the corresponding unit circuits of sense amplifier SA1 and furthermore to the corresponding unit circuits of data register DR1 of the serial access port.

Latches comprising two cross-connected CMOS inverter circuits are used as the basic structural elements of the unit circuits in sense amplifier SA1. Each of the said sense amplifier unit circuits is set in the operation mode by the timing signal ϕpa which is supplied by the timing control circuit TC, amplifies the micro-signals that are read from a memory cell and output to its corresponding complementary data line, and forms a binary signal with a high level or a low level.

The complementary common data line $\underline{CD}1$ to which the complementary data line that is specified by the Y address signals AY0 through AYi is selectively connected is connected to the input/output circuit RIO for the random access port. Complementary common data lines $\underline{CD}2$ through $\underline{CD}4$ which are provided corresponding to memory arrays M-ARY2 through M-ARY4 are similarly connected to the random access port input/output circuit RIO.

When the dual port memory is in the random access port write operation mode, the random input/output circuit RIO, which is set in the operation mode by the timing signal ϕrw supplied by the

timing control circuit TC, receives write data from an external device through input/output terminals IO1 through IO4 and transfers the said write data as complementary write signals to the complementary common data lines $\underline{C}D1$ through $\underline{C}D4$. Furthermore, when the dual port memory is in the random access port read operation mode, the random input/output circuit RIO, which is set in the operation mode by the timing signal ϕ_{RT} supplied by the timing control circuit TC, receives binary signals that are read from the memory cells over complementary common data lines $\underline{C}D1$ through $\underline{C}D4$, amplifies the said binary signals and then outputs the said binary signals from input/output terminals IO1 through IO4. Although not restricted by this, the said random input/output circuit RIO is provided with a logical operation circuit that uses the read/modify/write function to perform various [logical] operations between the input data and data read from the memory cells and then rewrites the results. The said logical operation circuit is provided with various [logical] operation modes for performing processes such as a raster operation.

The operation mode of the logical operation circuit is specified by the function control circuit FC which comprises a register for holding the operation codes which are supplied through external terminals A0 through A3 and a decoder which decodes the said operation codes and selects and specifies the operation mode of the logical operation circuit. When the level of the column address strobe signal $\overline{CAS}$ is set to low before the row address strobe signal $\overline{RAS}$ is, and if the level of the write enable signal $\overline{WE}$ is low at the same time, the operation codes are supplied to the dual port memory via external terminals A0 through A3. Furthermore, the specific combinations of the operation codes are used as internal control signal sp which sets the output of the serial input/output circuit SIO described hereinbelow in the so called x1 bit configuration.

As described hereinbelow, when the dual port memory is in the serial read operation mode, the external terminals IO1 through IO4 for data input and output are provided with the number of cycles of the serial clock signal SC required for starting the serial output operation after the serial read operation mode is activated. With the dual port memory of this embodiment, this arrangement allows the timing when the serial output mode will begin after its activation to be set at will and enables a serial output operation that is synchronized in a stable manner with the serial clock signal SC whose period will be short when the dot rate is high. The data on the number of cycles that is supplied to external data input/output terminals IO1 through IO4 is sent to timing control circuit TC as internal signals io1 through io4.

The serial access port of the dual port memory of this embodiment comprises data registers DR1 through DR4 of (n + 1) bits corresponding to the complementary data lines in each memory arrays, data selectors DSL1 through DSL4, pointer PNT, column address decoder SCD for the serial access port and serial input/output circuit SIO, the latter three being commonly provided for the aforesaid four data registers and data selectors. Incidentally, depending on the layout of the memory arrays on a semiconductor substrate, a plurality of pointers PNT and a plurality of the column address decoders SCD for the serial access port may be provided.

Corresponding to the complementary data lines in the memory array M-ARY1, the data register DR1 includes (n + 1) pieces of flip-flops for data latching purpose. Switch MOSFETs for data transfer use are provided between the input/output nodes of the said flip-flops and their corresponding noninverting signal line and inverting signal line of the complementary data lines. Timing signal ϕdt for data transfer use output by the timing control circuit TC is supplied to the gates of the aforesaid MOSFETs.

Each bit of the data register DR1 is connected to its corresponding switch MOSFET of data selector DSL1. The data selector DSL1, which is similarly constructed as the afore-described column switch SW1, selectively connects each bit of the data register DR1 with the complementary common data line $\overline{CDS1}$ used for serial input and output. The gates of each pair of switch MOSFETs of data selector DSL1 are commonly connected and are provided with the register selection signal from pointer PNT.

The pointer PNT comprises a latch circuit (pointer latch) which holds the serial operation start bit that is specified by the column address decoder SCD for the serial access port, shift register with (n + 1) bits, and a switch circuit consisting of an n-channel MOSFET that is provided between the aforesaid latch circuit and the aforesaid shift register. The output terminal ps for the last bit in the said shift register is connected to the input terminal for the first bit. Furthermore, the aforesaid timing signal ϕdt is commonly supplied to the gates of the aforesaid switch MOSFETs. When the dual port memory is in the serial input/output mode, the shift register of pointer PNT engages in a looping shift operation in accordance with the shift clock timing signal ϕc that is supplied by the timing control circuit TC. The selection signal that is held by the pointer latch circuit is supplied to the shifter register as its initial value when the level of the timing signal ϕdt becomes high.

The column address decoder SCD for the serial access port decodes the complementary internal address signals ay0 through ayi which are supplied by the column address buffer CADB and sets only the bit of pointer PNT corresponding to the first bit of the serial input/output specified by the Y address signals AY0 through AYi to a logical "1." To elaborate, when the serial input/output mode is being used, the word line is selected by the X address signals AX0 through AXi, and Y address signals AY0 through AYi specify the address of the first column where the serial input and output is to

be performed. The logical "1" signal that is written to the specified bit of pointer PNT by the column address decoder SCD for the serial access port is shifted in a loop inside pointer PNT in accordance with timing signal ϕc. The said shifting of the logical "1" signal results in a register selection signal with a high level to be sequentially supplied to the data selector DSL1. This then results in each bit of data register DR1 to be successively connected to the complementary common data line $\overline{CDS1}$ used for serial input and output. With the dual port memory of the present embodiment, this arrangement allows the serial input and output of the memory data to be started from any desired column address which in turn allows processes like scrolling on an image memory to be performed at a high speed.

In the foregoing manner, when the dual port memory is in the serial read operation mode, the $(n + 1)$ bits of read data that are output over $(n + 1)$ sets of complementary data lines in memory array M-ARY1 are stored in data register DR1 when the level of timing ϕdt becomes high. At the same time, with respect to pointer PNT, when the level of timing ϕdt becomes high, the selection signal that is held by the pointer latch is transferred to the shift register as the initial value. In accordance with the register selection signal that is successively sent from pointer PNT, read data is sent to the serial input/output circuit SIO via the complementary common data line $\overline{CDS1}$ for serial input and output. On the other hand, when the dual port memory is in the serial write operation mode, the write data which is serially sent from serial input/output terminal SIO1 via serial input/output circuit SIO is sequentially provided to the corresponding bit of the data register DR1 in accordance with the register selection signal that is successively sent from pointer PNT. When the level of timing ϕdt changes to high, the write data which was stored in data register DR1 is written, all at once, to the $(n + 1)$ pieces of memory cells which are connected to the selected word line in memory array M-ARY1.

The serial input/output circuit SIO includes a data input buffer, a data output buffer and four

main amplifiers which are provided corresponding to serial input/output terminals SIO1 through SIO4 and complementary common data lines $\overline{CDS1}$ through $\overline{CDS4}$ used for serial input and output. When the dual port memory is in the read data transfer mode, the data output buffer of the serial input/output circuit SIO is set in the operation mode when the level of the timing signal ϕsr from the timing control circuit TC becomes high, and the data that is output over the corresponding complementary common data lines $\overline{CDS1}$ through $\overline{CDS4}$ for serial input and output and then amplified by the corresponding main amplifiers is output to an external device using the serial input/output terminals SIO1 through SIO4. When the dual port memory is in the serial write operation mode, the data input buffer of the serial input/output circuit SIO is set in the operation mode when the level of the timing signal ϕsw from the timing control circuit TC becomes high, and the write data that is supplied from an external device over the corresponding serial input/output terminals SIO1 through SIO4 is transferred as complementary write data signals to the corresponding complementary common data lines $\overline{CDS1}$ through $\overline{CDS4}$ for serial input and output. The serial input/output circuit SIO performs the serial input and output operation on the memory data in accordance with timing signal ϕc which is generated by the timing control circuit TC based on a serial clock signal SC that is supplied from an external source.

As described above, with the dual port memory of this embodiment, the serial output signal of the serial input/output circuit SIO is ordinarily output four bits at a time using the four serial input/output terminals SIO1 through SIO4. However, to realize a serial memory with a larger memory capacity, it is possible to use the dual port memory as a memory with the so-called x1 bit configuration where data that is read and output from four memory arrays, M-ARY1 through M-ARY4, is serially output through one serial input/output terminal. In this case, as mentioned earlier, one of the combinations of the operation codes which control the operation mode of the logical operation

circuit in the random input/output circuit RIO is used as internal control signal sp which specifies a x1 bit configuration for the serial output. When the level of the said internal control signal sp from the function control circuit FC becomes high, a multiplexer that is provided in the serial input/output circuit SIO sequentially selects the read data that is serially output over the four sets of serial input/output complementary common data lines CDS1 through CDS4 and outputs to an external device using one serial input/output terminal SIO1. Since this serial output is performed in accordance with timing signal ϕc from the timing control circuit TC, the data rate becomes the same as what the data rate would be for each input/output terminal had the four serial input/output terminals SIO1 through SIO4 been used to perform a serial output four bits at a time.

The timing control circuit TC receives from an external source, as control signals, row address strobe signal $\overline{RAS}$, column address strobe signal $\overline{CAS}$, write enable signal $\overline{WE}$, data transfer control signal $\overline{DT/OE}$, and serial output control signal $\overline{SOE}$ and forms the various aforesaid timing signals and supplies them to the different circuits. The timing control circuit also uses the serial clock signal SC supplied from an external source to generate the timing signal ϕc which is used for synchronizing the serial input/output operation and supplies the said signal to the serial input/output circuit SIO.

The operation mode of the dual port memory is specified by suitably combining the various control signals. For example, if the level of the row address strobe signal $\overline{RAS}$ is low already and if, when the level of the column address strobe signal $\overline{CAS}$ becomes low, the level of the write enable signal $\overline{WE}$ is high, the ordinary read operation mode using the random access port is selected. If the

level of the row address strobe signal $\overline{RAS}$ is low already and if, when the level of the column address strobe signal $\overline{CAS}$ becomes low, the level of the write enable signal $\overline{WE}$ is low, the ordinary write operation mode using the random access port or the [logical] operation write operation mode is selected. Furthermore, if, when the level of the row address strobe signal $\overline{RAS}$ falls, the level of the write enable signal $\overline{WE}$ is high and the level of the data transfer control signal $\overline{DT/OE}$ is low, the read data in the memory array is transferred to data registers DR1 through DR4, and the so-called data transfer mode is selected for serially reading the data.

As described above, when the dual port memory of the present embodiment is in the data transfer mode, when the level of the row address strobe signal $\overline{RAS}$ falls to low, in synchrony with this change in level, the number of cycles of the serial clock signal SC required from activation until the start of the next data transfer operation on the serial read data is set in external terminals IO1 through IO4 used for data input and output. Because of this, the timing control circuit TC is provided with counter circuit CTR which receives the data on the number of cycles via the data input/output terminals IO1 through IO4 and performs a count-down operation in accordance with the serial clock signal SC. The read data that is output to the respective data lines is transferred to data registers DR1 through DR4 in accordance with the timing signal ϕdt which is generated when the value of counter circuit CTR in the timing control circuit TC becomes "0." The said data is then output by the serial input/output circuit SIO to the outside via serial input/output terminals SIO1 through SIO4 in accordance with the timing signal ϕc.

Next, if, when the level of the row address strobe signal $\overline{RAS}$ falls, the levels of the data transfer control signal $\overline{DT}/\overline{OE}$ and the write enable signal $\overline{WE}$ are both low and the level of the serial input/output control signal $\overline{SOE}$ is high, the timing control circuit TC sets the dual port memory in the serial write operation mode, and the serial write data that is supplied via serial input/output terminals SIO1 through SIO4 is fed to data registers DR1 through DR4. On the other hand, if, when the level of the row address strobe signal $\overline{RAS}$ falls, the levels of the data transfer control signal $\overline{DT}/\overline{OE}$ and the write enable signal $\overline{WE}$ are both low and the level of the serial input/output control signal $\overline{SOE}$ is also low, the write data transfer mode is selected, and the transfer timing signal ϕdt is generated. This sets the transfer switch MOSFETs of data registers DR1 through DR4 in an ON state. This results in the afore-described serial write operation mode, and the write data stored in data registers DR1 through DR4 are fed all at once to (n + 1) bits of memory cells that are connected to the selected word line in the memory array. The serial write operation using the serial access port of a dual port memory is realized by executing the write data transfer mode in combination after executing the afore-described serial write operation mode.

On the other hand, if the level of the column address strobe signal $\overline{CAS}$ changes from high to low before the level of the row address strobe signal $\overline{RAS}$ falls to low, the so-called $\overline{CAS}$ before $\overline{RAS}$ refresh mode is selected. Also, if the level of the write enable signal $\overline{WE}$ is already

low when the level of the row address strobe signal $\overline{RAS}$ falls, the [logical] operation mode setting cycle is selected, and the [logical] operation code which is supplied via external terminals A0 through A3 is stored in the register in the function control circuit FC.

With all of the operation modes other than the afore-described [logical] operation mode setting cycle, the X address signals AX0 through AXi which specify the word line are supplied to the external terminals A0 through Ai in synchrony with the falling level of the row address strobe signal $\overline{RAS}$. Also, if a particular operation mode requires a column address, the Y address signals AY0 through AYi which specify the complementary data line are supplied to external terminals A0 through Ai in synchrony with the falling level of the of the column address strobe signal $\overline{CAS}$.

Fig. 1 shows a circuit diagram of a part of one embodiment of the timing control circuit TC for a dual port memory shown in Fig. 2.

As previously stated, with the dual port memory of this embodiment, the data input/output external terminals IO1 through IO4 are used to specify, using a binary representation, the number of cycles of the serial clock signal SC that is required from the activation of the dual port memory by the level of the row address strobe signal $\overline{RAS}$ becoming low until the start of the data transfer operation on the read data. The said number of cycles is supplied as internal data io1 through io4 to the corresponding bits in the counter circuit CTR in the timing control circuit TC.

Another timing generating circuit is provided within timing control circuit TC, and from the said other timing generating circuit, the counter circuit CTR receives the timing signal ϕcs which is

generated in synchrony with the falling level of the row address strobe signal $\overline{RAS}$. The counter circuit CTR also receives the [counter] advancing timing signal ϕcp which is created within the timing control circuit TC shown in the said figure.

The inverted output signals $\overline{C1}$ through $\overline{C8}$ from each bit in the counter circuit CTR are supplied to the four input terminals of the AND gate circuit AG1. The level of the output signal ctr0 of the AND gate circuit AG1 is set to high when the inverted output signals $\overline{C1}$ through $\overline{C8}$ of the counter circuit CTR are all logical "0," that is, when the value of the counter circuit CTR becomes "0."

The output signal ctr0 of the AND gate circuit AG1 is fed to one input terminal of the NAND gate circuit NAG1 and, after the said output signal has been inverted by inverter circuit N3, also to one input terminal of the AND gate circuit AG2. The other input terminal of the NAND gate circuit NAG1 receives the output signal srm from a flip-flop which is not illustrated after the said output signal srm has passed through a suitable delay means (for example, an even number of inverter circuits). The said output signal srm from the flip-flop which is not illustrated is set if, when the level of the row address strobe signal $\overline{RAS}$ falls from high to low, the levels of the column address strobe signal $\overline{CAS}$ and the write enable signal $\overline{WE}$ are high and the level of the data transfer control signal $\overline{DT}$/$\overline{OE}$ is low. In other words, the output signal srm of the said flip-flop is used as a mode signal which specifies the read data transfer cycle of the dual port memory. Given this setup, the level of the output signal of the NAND gate circuit NAG1 becomes low when the levels of the output signal ctr0 of the AND gate circuit AG1 and the mode signal srm are high. The output signal of the NAND gate circuit

NAG1 is delayed by a suitable delay means D, inverted by inverter circuit N4 and then fed to one of the input terminals of the NOR gate circuit NOG1 while the output signal of the NAND gate circuit NAG1 is also fed directly to the other input terminal of the NOR gate circuit NOG1. The output signal of the NOR gate circuit NOG1 is fed to pointer PNT as timing signal ϕdt In other words, when the level of the mode signal srm is high which means that the dual port memory is in the read data transfer mode, the level of the timing signal ϕdt is temporarily set to high for a prescribed amount of time when the level of the output signal ctr0 of the AND gate circuit AG1 is high.

Serial clock signal SC that has passed through inverter circuits N1 and N2 is fed to the other input terminal of the AND gate circuit AG2. This means that the level of the output signal of the AND gate circuit AG2 becomes high when the level of the output signal ctr0 of the AND gate circuit AG1 is low, the level of the output signal of the inverter circuit N3 is high, that is, when the value of the counter circuit CTR is not "0," and the level of the serial clock signal SC is high. In other words, the output signal of the AND gate circuit AG2 serves as a timing signal ϕcp which advances and counts down the counter circuit CTR until the value of the counter circuit CTR becomes "0." Also, the serial clock signal SC that has passed through inverter circuits N1 and N2 becomes timing signal ϕc.

Fig. 3 shows a timing chart of one embodiment which is used to explain the operation of the read data transfer mode for a dual port memory that includes the timing control circuit TC shown in Fig. 4 [sic]. An overview of the read transfer mode of the dual port memory of this embodiment is explained with reference to Fig. 3.

In Fig. 3, the dual port memory is activated when the level of the row address strobe signal $\overline{\text{RAS}}$ changes from high to low. Prior to the level of the row address strobe signal $\overline{\text{RAS}}$ falling

from high to low, the levels of the column address strobe signal $\overline{CAS}$ and write enable signal $\overline{WE}$ are set to high, and the level of the data transfer control signal $\overline{DT}/\overline{OE}$ is set to low. The X address signals AX0 through AXi which specify the word line are fed to the external terminals A0 through Ai, and the number of serial clock signal SC cycles ctrz which must elapse between the level of the row address strobe signal $\overline{RAS}$ falling and the start of the serial output operation on the read data is fed to external terminals IO1 through IO4 used for data input and output.

The number of cycles ctrz is determined by the counter value of a counter circuit which is included in a memory control circuit that is external to the dual port memory and which is used for controlling the horizontal pixel location on a CTR [sic]. To explain, letting N1 represent the counter value corresponding to the last bit in one word line worth of read data and N2 represent the counter value when the level of the row address strobe signal $\overline{RAS}$ is to fall, the number of cycles ctrz is determined as follows:

$$ctrz = N1 - N2$$

The number cycles ctrz is set to a suitable value that satisfies the above equation while providing more time than is necessary to set a read data in the random access port of a dual port memory.

The level of the column address strobe signal $\overline{CAS}$ changes from high to low with a slight delay after the level of the row address strobe signal $\overline{RAS}$ falls. Prior to the level of the column address strobe signal $\overline{CAS}$ falling from high to low, the address of the data line that should be output

first during a serial output operation is supplied to external terminals A0 through Ai as Y address signals AY0 through AYi. The levels of the row address strobe signal $\overline{RAS}$, column address strobe signal $\overline{CAS}$, write enable signal $\overline{WE}$ and data transfer control signal $\overline{DT/OE}$ are returned to high after the counter value of the counter circuit CTR has become "0" and the serial output operation has been started.

With the dual port memory, when the level of the row address strobe signal $\overline{RAS}$ falls, the X address signals AX0 through AXi are stored in the row address buffer RADB, and a word line selection operation is performed. When the level of the row address strobe signal $\overline{RAS}$ falls, the level of the mode signal srm is set to high, the timing signal ϕcs is generated, and the number of cycles ctrz which is supplied to external terminals IO1 through IO4 used for data input and output are stored in the counter circuit CTR. This makes the output of the counter circuit CTR to a value other than "0," and the level of the output signal ctr0 of the AND gate circuit AG1 shown in Fig. 1 becomes low. When the level of the output signal of the said AND gate circuit AG1 becomes low, that is, when the level of the output signal of the inverter circuit N3 becomes high, the output signal of the AND gate circuit AG2, that is, the timing signal ϕcp for advancing the counter circuit CTR is generated. Whenever the level of the said timing signal ϕcp becomes low, the counter circuit CTR counts down from the value of the number of cycles ctrz that was initially stored toward the value of "0."

While the counter circuit CTR is counting down the serial clock signal SC, the word line selection operation is completed in the dual port memory, and the data that is read from the (n + 1) memory cells that are connected to the selected word line is set in their corresponding complementary

data lines. Also, when the level of the column address strobe signal $\overline{CAS}$ falls, the Y address signals AY0 through AYi are received, and the column address decoder SDC for the serial access port begins selecting a data line. At the same time that the said column address decoder SCD for the serial access port completes the decoding process, the timing signal ϕys is created, and a logical "1" is set in the bits of pointer PNT corresponding to the Y address signals AY0 through AYi.

As the counter circuit CTR counts down and when the counter value becomes "0," the level of the output signal ctr0 from the AND gate circuit AG1 becomes high which causes the level of the output signal of the inverter circuit N3 to become low and stops the timing signal ϕcp which is used for advancing the counter circuit CTR. Also, timing signal ϕdt is created and the read data that had been set in each of the data lines is transferred to data registers DR1 through DR4. Furthermore, timing signal ϕsr is generated in synchrony with the serial output control signal $\overline{SOE}$ which controls the data output buffer DOB of the serial input/output circuit SIO.

With the timing signal ϕsr at a high level, the serial input/output terminals SIO1 through SIO4 changes from a high-impedance state Hz to a level commensurate with the read data in the first address specified by Y address signals AY0 through AYi. This commences the output operation of the read data.

With the levels of the mode signal srm and the output signal ctr0 of the AND gate circuit AG1 being high, the timing control circuit TC generates timing signal ϕc which is used for shifting and is synchronized with the serial clock signal SC. The said timing signal ϕc is supplied to the serial input/output circuit SIO and the pointer PNT. This causes the logical "1" signal that had been set by the selection operation of the column address decoder SCD for the serial access port in the bits of

pointer PNT corresponding to the Y address signals AY0 through AYi to shift in a loop. This causes the read data that had been stored in data registers DR1 through DR4 to be output to serial input/output terminals SIO1 through SIO4 via the serial input/output circuit SIO and the complementary common data lines $\overline{CDS1}$ through $\overline{CDS4}$ for serial input/output use. The shifting of the pointer PNT with the timing signal ϕc happens in synchrony with the level of the said timing signal rising from low to high. The pointer PNT ignores the first pulse from the timing signal ϕc so as to secure an output time width for the first data.

As the serial output operation for the read data progresses as dictated by the timing signal ϕc and when the last read data is output, the level of the serial output control signal $\overline{SOE}$ is returned to high which causes the level of the mode signal srm to become low which, in turn, causes the level of the serial output timing signal ϕsr to be set to low in synchrony with the level of the serial clock signal SC rising to high. This stops the serial output operation of the dual port memory, and the serial input/output terminals SIO1 through SIO4 are set in a high-impedance state.

As the foregoing description shows, when the dual port memory of the present embodiment is in the read data transfer mode, the number of cycles ctrz of the serial clock signal SC required between the level of the row address strobe signal $\overline{RAS}$ becoming low and the start of the serial output operation of the read data is specified in synchrony with the level of the row address strobe signal $\overline{RAS}$ becoming low. The said number of cycles ctrz is set in the counter circuit CTR in the timing control circuit TC as an initial value for starting the count down operation. When the counting down by the counter circuit CTR ends and the counter value becomes "0," the serial output operation of the read data is begun. This allows the serial output operation of the dual port memory to be performed in

accurate synchrony with the serial clock signal SC and the scanning timing of the CTR [sic] and thereby provides stable displayed images even when an external high-resolution CTR [sic] with an extremely high dot rate for the displayed data is used.

As the foregoing description of the present embodiment shows, a semiconductor memory device such as a dual port memory that uses the present invention for image processing provides the following effects, namely:

(1) When a dual port memory is in the read data transfer mode, by specifying – in synchrony with the activation control signal – the number of cycles of the serial clock signal between the activation and the start of the serial output operation on the read data and by counting down using the counter circuit provided in the timing control circuit TC, the serial output operation on the read data can be started with a timing that is synchronized in a stable manner with the serial clock signal.

(2) Because of (1) above, a real time transfer of the read data can be performed in accurate synchrony with the serial clock signal SC and the scanning timing of the CTR [sic] and thereby provides stable displayed images even when an external high-resolution CTR [sic] with an extremely high dot rate for the displayed data is used.

The invention made by the inventor has been described hereinbefore in concrete terms using one embodiment of the invention, but the present invention is not restricted by the said embodiment. Needless to say, various modifications are possible without deviating from the gist of the invention For example, the timing control circuit TC of Fig. 1 coordinates the timing by performing a count down operation with the counter circuit CRT. However, it is also acceptable to store the number of cycles ctrz of the serial clock signal SC supplied from the outside in a register and to count up the counter circuit CTR and to start the serial output operation when the output of the counter circuit CTR matches

the number of cycles ctrz set in the register. It is also acceptable to decode the number of cycles ctrz, set a logical "1" in the corresponding bit of a separately provided shift register, shift the said shift register using the serial clock signal SC, and start the serial output operation when the said logical "1" has reached a prescribed position. With the present embodiment, the number of cycles ctrz is provided in synchrony with the falling level of the row address strobe signal $\overline{RAS}$, but it is also acceptable to do this in synchrony with the falling level of the column address strobe signal $\overline{CAS}$. Furthermore, it is acceptable for the dual port memory shown in Fig. 2 to comprise only one memory array or for the input/output circuit RIO for the random access port to be not provided with a logical operation circuit. In this manner, various modifications are possible in the block configuration, the combination of the control signals, etc. that are used.

Even though the description hereinbefore of the present invention was provided as applied to a dual port memory, the present invention is not restricted to use with dual port memories. For example, the present invention can be used with various multi-port memories with a serial input/output function. At the least, the present invention can be used with semiconductor memory devices whose serial output operation is controlled by control signals and a clock signal that are provided from an external source.

Effects of the invention

The effects that are obtained from the representative example of the invention disclosed in this application are as follows. To explain, when a dual port memory is in the read data transfer mode, by specifying the number of cycles of the serial clock signal between activation and the start of the data transfer operation on the read data and by counting down using the counter circuit provided in the

timing control circuit TC, the serial output operation on the read data can be started using a timing that is synchronized in a stable manner with the serial clock signal, and since a real time transfer of the read data can be performed in synchrony with the serial clock signal SC and the scanning timing of the CTR [sic], stable displayed images are obtained even when the dot rate of the displayed data is increased.

4 Brief description of the figures

Fig. 1 is a circuit diagram showing a part of one embodiment of a timing control circuit of a dual port memory that uses the present invention.

Fig. 2 is a block diagram showing one embodiment of a dual port memory that includes the timing control circuit shown in Fig. 1.

Fig. 3 is a timing chart of one embodiment of the read data transfer mode in a dual port memory shown in Fig. 2.

Fig. 4 is a timing chart for the read data transfer mode in a dual port memory which was developed by the inventor of the present application in concert with other individuals before the present invention.

TC:	Timing control circuit
CTR:	Counter circuit
AG1 through AG2:	AND gate circuits
NAG1:	NAND gate circuit
N1 through N4:	Inverter circuits
M-ARY1:	Memory array
SA1:	Sense amplifier
CSW1:	Column switch
RCD:	Column address decoder for the random access port

SCD:	Column address decoder for the serial access port
RADB:	Row address buffer
AMX:	Address muliplexer
CADB:	Column address buffer
REFC:	Refresh address counter
DR1:	Data register
DSL1:	Data selector
PNT:	Pointer
RIO:	Input/output circuit for the random access port
FC:	Function control circuit
SIO:	Input/output circuit for the serial access port

Agent: Patent agent Masao Ogawa [Seal: Illegible]

Fig. 1

Fig. 2

Fig. 3

Fig. 4

行の１９８６年３月２４日付「日経エレクトロニクス」の２４３頁～２６４頁に記載されている。

上記に記載されるデュアル・ポート・メモリには、記憶データを１ビット又は数ビット単位で入出力するためのランダム・アクセス・ポートと、記憶データをメモリアレイのワード線単位でシリアルに入出力するためのシリアル・アクセス・ポートが設けられる。

（発明が解決しようとする問題点）

このようなデュアル・ポート・メモリには、第４図に示すように、外部から供給される制御信号として、ロウアドレスストローブ信号$\overline{RAS}$、カラムアドレスストローブ信号$\overline{CAS}$及びライトイネーブル信号$\overline{WE}$のほかに、例えばデータ転送制御信号$\overline{DT}/\overline{OE}$、シリアル出力制御信号$\overline{SOE}$及びシリアルクロック信号ＳＣが設けられる。デュアル・ポート・メモリにおいて読み出しデータのシリアル出力動作が行われる読み出しデータ転送モードは、ロウアドレスストローブ信号$\overline{RAS}$がハイレベルからロウレベルに変化された時点で、カラムアドレスストローブ信号$\overline{CAS}$及びライトイネーブル信号$\overline{WE}$がハイレベルであり、データ転送制御信号$\overline{DT}/\overline{OE}$がロウレベルであることによって識別される。このとき、ロウアドレスストローブ信号$\overline{RAS}$の立ち下がりに同期して読み出しを行うワード線のアドレスＡＸが外部端子Ａ０～Ａｉに供給され、選択されたワード線に結合されるメモリセルからの読み出し信号が対応するデータ線に確立される。また、ロウアドレスストローブ信号$\overline{RAS}$にやや遅れてロウレベルとされるカラムアドレスストローブ信号$\overline{CAS}$の立ち下がりに同期してシリアル出力する先頭カラムアドレスＡＹが外部端子Ａ０～Ａｉに供給される。その後データ転送制御信号$\overline{DT}/\overline{OE}$がハイレベルに戻されることによって、各データ線にパラレルに出力された読み出しデータをシリアル・アクセス・ポートのデータレジスタに転送するためのタイミング信号ϕ_{tr}が形成されるとともに、シリアルクロック信号ＳＣに同期して形成されるタイミング信号ϕ_cに従ってデータレジスタに転送された新しいシリアルデータ（（ＡＸ・ＡＹ）以降のデータ）の出力動作が開始される。

データ転送制御信号$\overline{DT}/\overline{OE}$を一旦ロウレベルとした後、ハイレベルに戻してシリアル出力動作を開始させるタイミングは、このデュアル・ポート・メモリを駆動する外部のメモリ制御回路に設けられ水平画素位置を計数するためのカウンタ回路の出力信号をモニターすることによって制御される。すなわち、デュアル・ポート・メモリの１ワード線に結合されるメモリセルの読み出しデータの出力が終わりに近ずいた時点でデュアル・ポート・メモリの再起動が行われ、新しいワード線のメモリセルの読み出しデータが対応するデータ線に出力される。その後、メモリ制御回路のカウンタ回路の計数値が前回選択されたワード線に結合されるメモリセルからの読み出しデータのシリアル出力動作の末尾を示す値となり、シリアルクロック信号ＳＣがロウレベルとなる時間を見計らって、データ転送制御信号$\overline{DT}/\overline{OE}$がハイレベルに戻され、新しく選択されたワード線に結合されるメモリセルからの読み出しデータがデータレジスタに転送され、シリアル出力動作が開始される。これにより、ＣＲＴのドットレートに同期したリアルタイムなデータ転送が行われる。

しかしながら、ディスプレイ技術が進展し、高精彩のＣＲＴが開発されることによって、表示データがシリアル出力されるドットレートが高速化してきたため、データ転送制御信号$\overline{DT}/\overline{OE}$をシリアルクロック信号ＳＣに同期して立ち上げることが困難となってきた。すなわち、データ転送制御信号$\overline{DT}/\overline{OE}$をハイレベルに戻すタイミングは、前述のように、メモリ制御回路のカウンタ回路の出力信号をモニターすることで決定される。したがって、シリアルクロック信号ＳＣによってカウンタ回路が歩進する遅延時間とその出力信号をデコードしてモニターする遅延時間が、シリアルクロック信号ＳＣの周期に比較して相対的に大きくなると、データ転送制御信号$\overline{DT}/\overline{OE}$をシリアルクロック信号ＳＣに同期して立ち上げることが困難となるものである。このため、第４図に

いて同期信号として用いられるシリアルクロック信号ＳＣが入力される。

この実施例のデュアル・ポート・メモリのランダム・アクセス・ポートには、特に制限されないが、４つのメモリアレイＭ－ＡＲＹ１～Ｍ－ＡＲＹ４が設けられ、それぞれのメモリアレイに対応してセンスアンプＳＡ１～ＳＡ４、カラムスイッチＣＳＷ１～ＣＳＷ４が設けられる。また、メモリアレイＭ－ＡＲＹ１～Ｍ－ＡＲＹ４に共通に、ランダム・アクセス・ポート用カラムアドレスデコーダＲＣＤ及びロウアドレスデコーダＲＤが設けられる。これらのアドレスデコーダは、半導体基板上のメモリアレイの配置に応じて、複数個設けられることもある。第２図には、メモリアレイＭ－ＡＲＹ１とその周辺回路が例示的に示されている。

第２図において、メモリアレイＭ－ＡＲＹ１は、同図の垂直方向に配置されるｍ＋１本のワード線と、同図の水平方向に配置されるｎ＋１組の相補データ線及びこれらのワード線と相補データ線の交点に配置される（ｍ＋１）×（ｎ＋１）個のメモリセルにより構成される。

メモリアレイＭ－ＡＲＹ１を構成するダイナミック型メモリセルは、情報蓄積用キャパシタとアドレス選択用ＭＯＳＦＥＴにより構成される。同一の行に配置されるｎ＋１個のメモリセルのアドレス選択用ＭＯＳＦＥＴのゲートは、対応するワード線に結合される。各ワード線は、さらにロウアドレスデコーダＲＤに結合され、Ｘアドレス信号ＡＸ０～ＡＸｉに指定される一本のワード線が選択・指定される。

ロウアドレスデコーダＲＤは、ロウアドレスバッファＲＡＤＢから供給される相補内部アドレス信号a_{x0}～a_{xi}（ここで、例えば外部から供給されるＸアドレス信号ＡＸ０と同相の内部アドレス信号a_{x0}と正相の内部アドレス信号$\overline{a_{x0}}$をあわせて相補内部アドレス信号a_{x0}のように表す。以下同じ）をデコードし、Ｘアドレス信号ＡＸ０～ＡＸｉに指定される一本のワード線を選択し、ハイレベルの選択状態とする。ロウアドレスデコーダＲＤによるワード線の選択動作は、タイミング制御回路ＴＣから供給されるワード線選択タイミング信号ϕ_xに従って行われる。

ロウアドレスバッファＲＡＤＢは、アドレスマルチプレクサＡＭＸから供給されるロウアドレス信号を受け、相補内部アドレス信号a_{x0}～a_{xi}を形成して、ロウアドレスデコーダＲＤに供給する。この実施例のダイナミック型ＲＡＭでは、ロウアドレスを指定するためのＸアドレス信号ＡＸ０～ＡＸｉとカラムアドレスを指定するためのＹアドレス信号ＡＹ０～ＡＹｉは、同一の外部端子Ａ０～Ａｉを介して時分割されて供給されるいわゆるアドレスマルチプレクス方式を採っている。したがって、外部から制御信号として供給されるロウアドレスストローブ信号$\overline{RAS}$の立ち下がりに同期してＸアドレス信号ＡＸ０～ＡＸｉが、またカラムアドレスストローブ信号$\overline{CAS}$の立ち下がりに同期してＹアドレス信号ＡＹ０～ＡＹｉがそれぞれ外部端子Ａ０～Ａｉに供給される。さらに、この実施例のダイナミック型ＲＡＭには、メモリセルの記憶データを所定の周期内に読み出し・再書き込みするための自動リフレッシュモードが設けられ、この自動リフレッシュモードにおいてリフレッシュすべきワード線を指定するためのリフレッシュアドレスカウンタＲＥＦＣが設けられる。

アドレスマルチプレクサＡＭＸは、タイミング制御回路ＴＣから供給されるタイミング信号ϕ_{ref}に従って、外部端子Ａ０～Ａｉを介して供給されるＸアドレス信号ＡＸ０～ＡＸｉとリフレッシュアドレスカウンタＲＥＦＣから供給されるリフレッシュアドレス信号c_{x0}～c_{xi}を選択し、ロウアドレス信号としてロウアドレスバッファＲＡＤＢに伝達する。すなわち、タイミング信号ϕ_{ref}がロウレベルとされる通常のメモリアクセスモードにおいて、外部端子Ａ０～Ａｉを介して外部の装置から供給されるＸアドレス信号ＡＸ０～ＡＸｉを選択し、タイミング信号ϕ_{ref}がハイレベルとされる自動リフレッシュモードにおいて、リフレッシュアドレスカウンタＲＥＦＣから出力

されるタイミング信号φrrによって動作状態とされ、相補共通データ線$\overline{CD1}$～$\overline{CD4}$を介して伝達されるメモリセルの読み出し2値信号をさらに増幅し、入出力端子I01～I04から送出する。さらに、このランダム入出力回路RIOには、特に制限されないが、リード・モディファイ・ライト動作を用いて、メモリセルから読み出したデータと入力データとの間で種々の演算を行い再度書き込むための論理演算回路が設けられる。この論理演算回路には、ラスタ演算等の処理を行うための各種の演算モードが用意される。

論理演算回路の演算モードは、機能制御回路FCによって指定される。機能制御回路FCは、外部端子A0～A3を介して供給される演算コードを保持するためのレジスタと、その演算コードをデコードし論理演算回路の演算モードを選択・指定するためのデコーダを含む。演算コードは、カラムアドレスストローブ信号$\overline{CAS}$がロウアドレスストローブ信号$\overline{RAS}$に先立ってロウレベルとされ、同時にライトイネーブル信号$\overline{WE}$がロウレベルとされる組み合わせにおいて、外部端子A0～A3を介してデュアル・ポート・メモリに供給される。また、演算コードの特定の組み合わせは、後述するシリアル入出力回路SIOの出力をいわゆる×1ビット構成とするための内部制御信号φとして用いられる。

データ入出力用外部端子I01～I04には、後述するように、デュアル・ポート・メモリのシリアル読み出し動作モードにおいて、起動後シリアル出力動作を開始するまでの間のシリアルクロック信号SCのサイクル数が入力される。これにより、この実施例のデュアル・ポート・メモリは、起動後シリアル出力動作を開始するタイミングを任意に設定することができ、高速ドットレートに対応して短い周期とされるシリアルクロック信号SCに設定して同期化されたシリアル出力動作を行うことができる。データ入出力用外部端子I01～I04に入力されるサイクル数は、内部信号i01～i04として、タイミング制御回路TCに送られる。

一方、この実施例のデュアル・ポート・メモリのシリアル・アクセス・ポートは、各メモリアレイの相補データ線に対応して設けられるn+1ビットのデータレジスタDR1～DR4と、データセレクタDSL1～DSL4及びこれらの4つのデータレジスタとデータセレクタに共通に設けられるポインタPNT、シリアル・アクセス・ポート用カラムアドレスデコーダSCD及びシリアル入出力回路SIOによって構成される。なお、ポインタPNT及びシリアル・アクセス・ポート用カラムアドレスデコーダSCDは、半導体基板上におけるメモリアレイの配置の関係で複数個設けられることもある。

データレジスタDR1は、メモリアレイM-ARY1の各相補データ線に対応して設けられるデータラッチ用のn+1個のフリップフロップを含む。これらのフリップフロップの入出力ノードと対応する相補データ線の非反転信号線及び反転信号線の間には、データ転送用のスイッチMOSFETがそれぞれ設けられ、そのゲートにはタイミング制御回路TCからデータ転送用のタイミング信号φtrが供給される。

データレジスタDR1の各ビットは、さらにデータセレクタDSL1の対応するスイッチMOSFETに結合される。データセレクタDSL1は、上述のカラムスイッチCSW1と同様な構成とされ、データレジスタDR1の各ビットとシリアル入出力用相補共通データ線$\overline{CDS1}$を選択的に接続する。データセレクタDSL1の各対のスイッチMOSFETのゲートはそれぞれ共通接続され、ポインタPNTからレジスタ選択信号が供給される。

ポインタPNTは、シリアル・アクセス・ポート用カラムアドレスデコーダSCDによって指定されるシリアル動作開始ビットを保持するラッチ回路（ポインタラッチ）と、n+1ビットのシフトレジスタ及びこれらの間に設けられるNチャンネルMOSFETからなるスイッチ回路とにより構成される。シフトレジスタの最終ビットの出力端子pnはその先頭ビットの入力端子に結合され

るシリアル入出力用相補共通データ線$\overline{C}$DS1～$\overline{C}$DS4に伝達する。シリアル入出力回路SIOの記憶データにおけるシリアル入出力動作は、タイミング制御回路TCにおいて外部から供給されるシリアルクロック信号SCをもとに形成されるタイミング信号φcに従って行われる。

この実施例のデュアル・ポート・メモリでは、通常シリアル入出力回路SIOのシリアル出力信号は、上記のように4つのシリアル入出力端子SIO1～SIO4を介して4ビット同時に出力される。しかし、さらに記憶容量の大きなシリアルメモリを実現したい場合、このデュアル・ポート・メモリを、4つのメモリアレイM-ARY1～M-ARY4から出力される読み出しデータを一つのシリアル入出力端子を介してシリアルに出力するいわゆる×1ビット構成のメモリとして用いることができる。この場合、前述のように、ランダム入出力回路RIOの論理演算回路の演算モードを制御するための演算コードの組み合わせの一つが、シリアル出力を×1ビット構成とするための内部制御信号φpとされる。シリアル入出力回路SIOは、通信制御回路FCから供給される内部制御信号φpがHイレベルになると、4組のシリアル入出力用相補共通データ線$\overline{C}$DS1～$\overline{C}$DS4を介してそれぞれシリアルに出力される読み出しデータを、シリアル入出力回路SIO内に設けられるマルチプレクサによって順次選択し、一つのシリアル入出力端子SIO1を介して外部の装置に出力する。このシリアル出力は、タイミング制御回路TCから供給されるタイミング信号φcに従って行われるため、4つのシリアル入出力端子SIO1～SIO4によって同時に4ビットのシリアル出力が行われる場合の各入出力端子のデータレートと同じデータレートとなる。

タイミング制御回路TCは、外部から制御信号として供給されるロウアドレスストローブ信号$\overline{RAS}$、カラムアドレスストローブ信号$\overline{CAS}$、ライトイネーブル信号$\overline{WE}$、データ転送制御信号$\overline{DT}$／$\overline{OE}$及びシリアル出力制御信号SOEによって、上記各種のタイミング信号を形成し、各回路に供給する。また、外部から供給されるシリアルクロック信号SCにより、シリアル入出力動作を同期化するためのタイミング信号φcを形成し、シリアル入出力回路SIOに供給する。

各制御信号が適当な組み合わせとされることで、デュアル・ポート・メモリの動作モードが指定される。例えば、まずロウアドレスストローブ信号$\overline{RAS}$がロウレベルとなり、続いてカラムアドレスストローブ信号$\overline{CAS}$がロウレベルとなる時点でライトイネーブル信号$\overline{WE}$がハイレベルであると、通常のランダム・アクセス・ポートの読み出し動作モードとされる。ロウアドレスストローブ信号$\overline{RAS}$がロウレベルとなり、続いてカラムアドレスストローブ信号$\overline{CAS}$がロウレベルとなる時点でライトイネーブル信号$\overline{WE}$がロウレベルである場合、通常のランダム・アクセス・ポートの書き込み動作モードあるいは演算書き込み動作モードとされる。さらに、ロウアドレスストローブ信号$\overline{RAS}$の立ち下がり時点でライトイネーブル信号$\overline{WE}$がハイレベルでありデータ転送制御信号$\overline{DT}$／$\overline{OE}$がロウレベルの場合、メモリアレイの読み出しデータをデータレジスタDR1～DR4に転送しいわゆるシリアル読み出しを行うための読み出しデータ転送モードとされる。

前述のように、この実施例のデュアル・ポート・メモリの読み出しデータ転送モードでは、ロウアドレスストローブ信号$\overline{RAS}$のロウレベルへの立ち下がりに同期して、データ入出力用外部端子IO1～IO4に記憶装置のシリアル読み出しデータのデータ転送動作を開始するまでのシリアルクロック信号SCのサイクル数が指定される。このため、タイミング制御回路TCには、データ入出力端子IO1～IO4を介して入力されるサイクル数を取り込み、シリアルクロック信号SCに従ってカウントダウンするためのカウンタ回路CTRが設けられる。各データ線に出力された読み出しデータは、タイミング制御回路TCのカウンタ回路CTRの計数値が"0"となることによって形成されるタイミング信号φdによってデータレジスタDR1～DR4に転送され、さらにタイ

方の入力端子には、ロウアドレスストローブ信号$\overline{RAS}$のハイレベルからロウレベルへの立ち下がりにおいて、カラムアドレスストローブ信号$\overline{CAS}$及びライトイネーブル信号$\overline{WE}$がハイレベルとされかつデータ転送制御信号$\overline{DT}/\overline{OE}$がロウレベルとされることでセットされる図示されないフリップフロップの出力信号trmが、適当な遅延手段（例えば偶数個のインバータ回路）Dを介して供給される。つまり、このフリップフロップの出力信号trmは、デュアル・ポート・メモリの読み出しデータ転送サイクルを指定するためのモード信号として用いられる。これにより、ナンドゲート回路NAG1の出力信号は、アンドゲート回路AG1の出力信号$ctr0$とモード信号trmがハイレベルである時にロウレベルとなる。ナンドゲート回路NAG1の出力信号は、一方において、適当な遅延手段Dによって遅延されさらにインバータ回路N4によって反転された後、ノアゲート回路NOG1の一方の入力端子に入力される。また、ナンドゲート回路NAG1の出力信号は、他方において、そのままノアゲート回路NOG1の他方の入力端子に入力される。ノアゲート回路NOG1の出力信号は、タイミング信号ϕdtとしてポインタPNTに供給される。つまり、このタイミング信号ϕdtは、モード信号trmがハイレベルとされるデュアル・ポート・メモリの読み出しデータ転送モードにおいて、アンドゲート回路AG1の出力信号$ctr0$がハイレベルとされると共に、所定の期間だけ一時的にハイレベルとされるものとなる。

一方、アンドゲート回路AG2の他方の入力端子には、インバータ回路N1及びN2を介してシリアルクロック信号SCが供給される。これにより、アンドゲート回路AG2の出力信号は、アンドゲート回路AG1の出力信号$ctr0$がロウレベルでインバータ回路N3の出力信号がハイレベルすなわちカウンタ回路CTRの計数値が"0"でなく、シリアルクロック信号SCがハイレベルであるときに、ハイレベルとなる。つまり、アンドゲート回路AG2の出力信号は、カウンタ回路CTRの計数値が"0"に達するまでカウンタ回路CTRをカウントダウンさせるための多重用タイミング信号ϕcpとなる。また、インバータ回路N1及びN2を通ったシリアルクロック信号SCは、タイミング信号ϕcとなる。

第3図には、第4図のタイミング制御回路TCを含むデュアル・ポート・メモリの読み出しデータ転送モードにおける動作を説明するための一実施例のタイミング図が示されている。この図により、この実施例のデュアル・ポート・メモリの読み出し転送モードの概要を説明する。

第3図において、このデュアル・ポート・メモリは、ロウアドレスストローブ信号$\overline{RAS}$がハイレベルからロウレベルに変化されることによって起動される。このロウアドレスストローブ信号$\overline{RAS}$の立ち下がりに先立って、カラムアドレスストローブ信号$\overline{CAS}$及びライトイネーブル信号$\overline{WE}$がハイレベルとされ、データ転送制御信号$\overline{DT}/\overline{OE}$がロウレベルとされる。また、外部端子A0～Aiにはワード線を指定するためのXアドレス信号AX0～AXiが供給され、データ入出力用外部端子I01～I04にはロウアドレスストローブ信号$\overline{RAS}$の立ち下がりから読み出しデータのシリアル出力動作を開始するまでのシリアルクロック信号SCのサイクル数$ctrz$が供給される。

このサイクル数$ctrz$は、デュアル・ポート・メモリの外部に設けられるメモリ制御回路に含まれCTRの水平帰線位置を制御するためのカウンタ回路の計数値に従って決定される。すなわち、1ワード線分の読み出しデータの末尾ビットに対応する計数値をN1とし、ロウアドレスストローブ信号$\overline{RAS}$を立ち下げる時点での計数値をN2とするとき、サイクル数$ctrz$は、

$$ctrz=N1-N2$$

として求められる。このサイクル数$ctrz$は、以上の式を満足し、かつデュアル・ポート・メモリのランダム・アクセス・ポートにおいて読み出しデータが確立されるまでの時間を越える範囲で、適当な値に決定される。

CDS1～CDS4及びシリアル入出力回路SIOを介してシリアル入出力端子SIO1～SIO4に出力される。タイミング信号φcによるポインタPNTのシフト動作は、タイミング信号のロウレベルからハイレベルへの立ち上がりに同期して行われる。また、ポインタPNTにおいて、タイミング信号φcの先頭パルスは回復され、先頭データの出力時間幅が確保される。

タイミング信号φcによる読み出しデータのシリアル出力動作が進み、全ての読み出しデータの出力が終了すると、シリアル出力制御信号$\overline{SOE}$がハイレベルに戻される。このシリアル出力制御信号$\overline{SOE}$のハイレベルによって、モード信号r_mがロウレベルとされ、シリアル出力用のタイミング信号ϕ_{sr}がシリアルクロック信号SCの立ち上がりに同期してロウレベルとされる。これにより、デュアル・ポート・メモリのシリアル出力動作は停止され、シリアル入出力端子SIO1～SIO4はハイインピーダンス状態とされる。

以上のように、この実施例のデュアル・ポート・メモリでは、読み出しデータ転送モードにおいて、ロウアドレスストローブ信号$\overline{RAS}$の立ち下がりに同期して、ロウアドレスストローブ信号$\overline{RAS}$の立ち下がりから読み出しデータのシリアル出力動作を開始するまでの間のシリアルクロック信号SCのサイクル数c_{ir}が指定される。このサイクル数c_{ir}は、タイミング制御回路TCに設けられるカウンタ回路CTRに初期セットされ、カウントダウンが行われる。カウンタ回路CTRによるカウントダウンが終了し、その計数値が"0"になった時点で、読み出しデータのシリアル出力動作が開始される。このため、外部に設けられるCTRが高速化され、表示データのドットレートが非常に高速化されているにもかかわらず、シリアルクロック信号SCとCTRのスキャンタイミングに確実に同期してデュアル・ポート・メモリのシリアル出力動作が行われ、安定した表示画像を得ることができるものである。

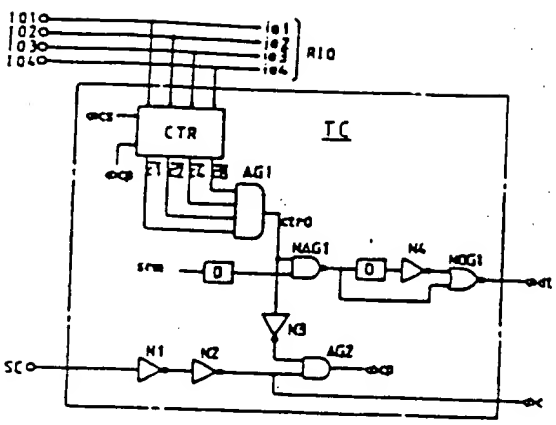
以上の本実施例に示されるように、この発明を画像処理用メモリとして用いられるデュアル・ポート・メモリ等の半導体記憶装置に適用した場合、次のような効果が得られる。すなわち、

(1)デュアル・ポート・メモリの読み出しデータ転送モードにおいて、転送制御信号に同期して、転送後から読み出しデータのシリアル出力動作を開始するまでの間のシリアルクロック信号のサイクル数を指定し、タイミング制御回路TCに設けられるカウンタ回路によってカウントダウンすることで、シリアルクロック信号に同期し安定したタイミングで読み出しデータのシリアル出力動作を開始することができるという効果が得られる。

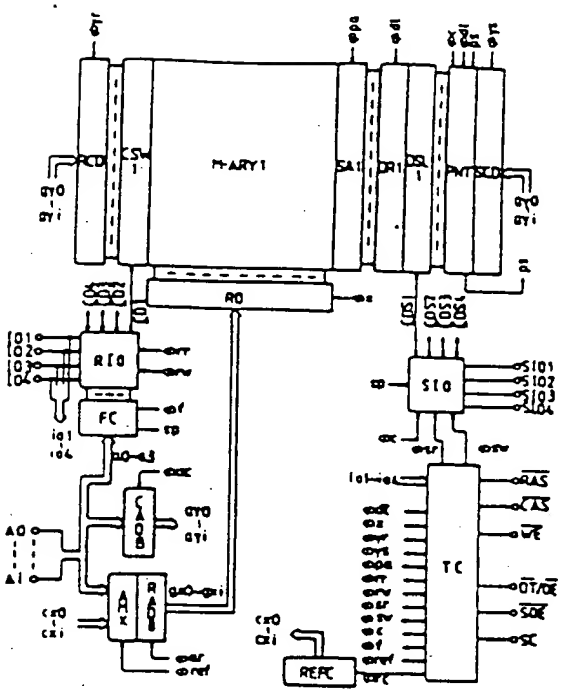
(2)上記(1)項により、外部に設けられるCTRが高精細化され、表示データのドットレートが非常に高速化されているにもかかわらず、シリアルクロック信号SC及びCTRのスキャンタイミングに確実に同期して読み出しデータのリアルタイム転送を行うことができ、安定した表示画像を得ることができるという効果が得られる。

以上本発明者によってなされた発明を実施例に基づき具体的に説明したが、この発明は上記実施例に限定されるものではなく、その要旨を逸脱しない範囲で種々変更可能であることはいうまでもない。例えば、第1図のタイミング制御回路TCでは、カウンタ回路CTRをカウントダウンすることによってタイミング整合を行っているが、外部から供給されるシリアルクロック信号SCのサイクル数c_{ir}をレジスタに保持するとともにカウンタ回路CTRをカウントアップさせ、カウンタ回路CTRの出力とレジスタにセットされるサイクル数c_{ir}とが一致したときにシリアル出力動作を開始させるようにしてもよい。また、サイクル数c_{ir}をデコードし、到達後設けられるシフトレジスタの対応するビットに論理"1"をセットした後、シリアルクロック信号SCによってシフトレジスタをシフトさせ、この論理"1"が所定の位置に達したことによってシリアル出力動作を開始させる方法もよい。この実施例では、サイクル数c_{ir}をロウアドレスストローブ信号$\overline{RAS}$の立ち下がりに同期して供給しているが、カラムアドレスストローブ信号$\overline{CAS}$の立ち下が

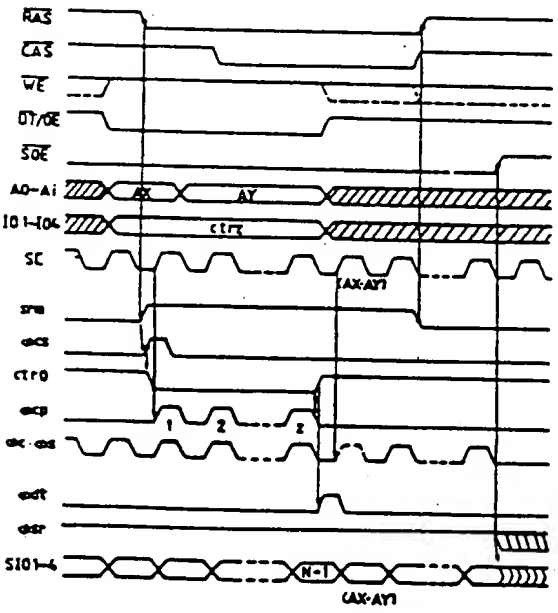
第 1 図



第 2 図



第 3 図



第 4 図